AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application. The following listing provides the amended claims with the amendments marked with deleted material crossed out and new material underlined to show the changes made.

Claims 1 – 57. (Canceled)

58.   (Previously Presented) For an electronic-design-automation placer that uses a set of partitioning lines, that define a plurality of slots, to partition an integrated-circuit ("IC") layout region into a plurality of sub-regions corresponding to said slots, wherein a plurality of line paths exist between said slots, a method of pre-computing attributes that are used for placing circuit modules in an IC layout region, the method comprising:

a)   for each combination of said slots, identifying at least one connection graph that represents a topology of interconnect lines necessary for connecting the combination of said slots;

b)   for each combination of said slots, identifying the line paths used by the at least one connection graph for that particular combination of slots, wherein a plurality of the identified line paths are diagonal; and

c)   storing the plurality of identified line paths for each combination of slots in a storage structure, wherein said stored line paths are used by the placer to compute costs associated with different placements of said circuit modules.

59.   (Previously Presented) The method of claim 58, wherein a plurality of the line paths are horizontal, and a plurality are vertical.

60.   (Currently Amended) The method of claim 58, wherein the <u>at least one</u> connection ~~graphs are Steiner trees~~ <u>graph is a Steiner tree</u>.

61.   (Currently Amended) The method of claim 58, wherein the <u>at least one</u> connection ~~graphs are~~ <u>is a</u> minimum spanning ~~trees~~ <u>tree</u>.

62.   (Previously Presented) The method of claim 58, wherein the at least one connection graph is determined to be optimal based on at least one particular selection criterion.

63.   (Previously Presented) The method of claim 62, wherein identifying the line paths comprises identifying the line paths used by all optimal connection graphs for each combination of said slots.

64.   (Currently Amended) The method of claim 58, wherein the at least one particular selection criterion is the length of the <u>at least one</u> connection ~~graphs~~ <u>graph</u>.

65.   (Currently Amended) The method of claim 64, wherein another selection criterion for determining whether the at least one connection ~~graphs are~~ graph is optimal is the number of bends of the at least one connection ~~graphs~~ graph.

66.   (Original) The method of claim 58, wherein the line paths are defined based on a wiring model for the IC layout and on a partitioning structure defined by the partitioning lines.

67.   (Previously Presented) For an electronic-design-automation placer that uses a set of partitioning lines, that define a plurality of slots, to partition an integrated-circuit ("IC") layout region into a plurality of sub-regions corresponding to said slots, wherein a plurality of edges exist between said slots, a method of pre-computing attributes that are used for placing circuit modules in an IC layout region, the method comprising:

a)   for each combination of said slots, identifying at least one connection graph that represents a topology of interconnect lines necessary for connecting the combination of said slots;

b)   for each combination of said slots, identifying the edges intersected by the at least one connection graph for that particular combination of slots, wherein a plurality of the identified edges are diagonal; and

c)   storing the plurality of identified edges for each combination of slots in a storage structure, wherein said stored edges are used by the placer to compute costs associated with different placements of said circuit modules.

68.   (Previously Presented) The method of claim 67, wherein a plurality of the edges are horizontal, and a plurality are vertical.

69.   (Currently Amended) The method of claim 67, wherein the at least one connection ~~graphs are Steiner trees~~ graph is a Steiner tree.

70.   (Currently Amended) The method of claim 67, wherein the at least one connection ~~graphs are minimum spanning trees~~ graph is a minimum spanning tree.

71.   (Currently Amended) The method of claim 67, wherein the at least one connection ~~graphs are~~ graph is determined to be optimal based on at least one particular selection criterion.

72.   (Previously Presented) The method of claim 71, wherein identifying the edges comprises identifying the edges intersected by all optimal connection graphs for each combination of said slots.

73.   (Currently Amended) The method of claim 72, wherein the selection criterion is the length of the at least one connection ~~graphs.~~ graph.

74.   (Currently Amended) The method of claim 73, wherein another selection criterion for determining whether the at least one connection ~~graphs are optimal~~ graph is optimal, is the number of bends of the connection ~~graphs~~ graph.

75.   (Original) The method of claim 67, wherein the edges are defined based on a wiring model for the IC layout and on a partitioning structure defined by the partitioning lines.